**Ficha 7**

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| **Flip-Flop JK ms, com base em (FF rs) com CLEAR PRESET (CLR PR)** |
| 1. Completa os espaços em branco |
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| A imagem representa um Flip-Flop do tipo Flip-Flop \_\_ \_\_, com base em (FF rs) com CLEAR \_\_\_\_\_\_ (CLR PR) com portas \_\_\_\_\_  J significa SET e K significa \_\_\_\_\_\_\_, ou seja, K Desliga a saída Q e J \_\_\_\_ a saída Q.  CLEAR pode ser representado por CLR e faz \_\_\_\_\_\_ ao circuito independentemente do estado das estradas J, K e CLK.  PRESET pode ser representado por \_\_\_\_ e faz SET ao circuito independentemente do estado das estradas J, K e CLK.  Quando PR e CLR estão em 0 o circuito entra em \_\_\_\_\_\_\_ \_\_\_\_\_\_\_.  Podemos dizer que as entradas CLR e PR “mandam” no circuito. ⃝ Verdadeiro ou ⃝ falso.  Se o estado de PR’ e CLR’ for 1, a transição do Clock permite \_\_\_\_\_\_\_\_ o MASTER e \_\_\_\_\_\_\_ o SLAVE ou \_\_\_\_\_\_\_\_\_ o MASTER e \_\_\_\_\_\_\_\_\_ o Slave.  Este circuito entra em memória quando: CLR=1, PR=1, J=0, K=0 ou quando CLK=0 ou CLK=1  Os FFjkMS funcionam na subida ou descida do Clok. Um FF que funciona pela borda de subida diz-se de transição positiva, um FF que funciona na borda de descida diz-se de transição \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |

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| 2. Preenche a tabela de verdade   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Entradas** | | | | | | **Saídas** | | | **Estado** | | | CLK | J | K | **PR’** | **CLR’** | Q | | Q’ |  | | | x | x | x | 0 | 0 |  | |  |  | | | x | x | x | 0 | 1 |  | |  |  | | | x | x | x | 1 | 0 |  | |  |  | | | 0/1 | x | x | 1 | 1 |  | |  |  | | | ˄ | 0 | 0 | 1 | 1 |  | |  |  | | | ˄ | 0 | 1 | 1 | 1 |  | |  |  | | | ˄ | 1 | 0 | 1 | 1 |  | |  |  | | | ˄ | 1 | 1 | 1 | 1 |  | |  |  | | | Clear = CLR faz RESET ao circuito  Preset = PR faz SET ao circuito | | |
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